

- 1 What is claimed is:
- 2 1. A package substrate for improving electrical performance comprising:
- 3 a first insulating layer having a top surface and a bottom surface;
- 4 a plurality of groups of inner fingers formed on the top surface of the first insulating
- 5 layer for electrically connecting to a chip;
- 6 a plurality of outer fingers formed on the top surface of the first insulating layer for
- 7 electrically connecting to the chip;
- 8 a plurality of outer through holes formed through the first insulating layer and
- 9 electrically connected to the corresponding outer fingers;
- 10 a plurality of inner through holes formed through the first insulating layer and
- 11 electrically connected to the corresponding inner fingers; and
- 12 a ground/power layer disposed on the bottom surface of the first insulating layer,
- 13 wherein the ground/power layer has a plurality of openings, and the inner through
- 14 holes are crowded in groups to pass through the openings which are electrically
- 15 isolated from the ground/power layer.
- 16 2. The substrate in accordance with claim 1, wherein a distance between the two adjacent
- 17 openings is not less than 0.2mm.
- 18 3. The substrate in accordance with claim 1, wherein the ground/power layer between
- 19 two adjacent openings is in strip shape.
- 20 4. The substrate in accordance with claim 1, wherein each group of inner through holes
- 21 pass through the corresponding openings and arranged in grid array.
- 22 5. The substrate in accordance with claim 1, wherein the top surface of the first insulating
- 23 layer includes a chip-attaching region.
- 24 6. The substrate in accordance with claim 5, wherein the openings are radially oriented to
- 25 the chip-attaching region.
- 26 7. The substrate in accordance with claim 5, further comprising a metal ring formed on
- 27 the top surface of the first insulating layer between the chip-attaching region and the

- 1 inner fingers.
- 2 8. The substrate in accordance with claim 1, further comprising a second insulating layer
3 formed on the bottom surface of the first insulating layer to sandwich the
4 ground/power layer.
- 5 9. The substrate in accordance with claim 8, further comprising another ground/power
6 layer on the bottom surface of the second insulating layer.
- 7 10. A package substrate for improving electrical performance comprising:
8 a first insulating layer having a top surface and a bottom surface;
9 a plurality of inner fingers formed on the top surface of the first insulating layer for
10 electrically connecting a chip;
11 a plurality of outer fingers formed on the top surface of the first insulating layer for
12 electrically connecting the chip;
13 a plurality of outer through holes formed through the first insulating layer and
14 electrically connected with corresponding outer fingers;
15 a plurality of inner through holes formed through the first insulating layer and
16 electrically connected with corresponding inner fingers; and
17 a first ground/power layer disposed on the bottom surface of the first insulating layer,
18 wherein the first ground /power layer has a plurality of openings, at least one of the
19 inner through holes passes through each opening with electrical isolation from the first
20 ground/power layer in a manner that the openings are crowded in groups for improving
21 electrical performance.
- 22 11. The substrate in accordance with claim 10, wherein the first ground/power layer
23 between two adjacent groups of the openings is in strip shape.
- 24 12. The substrate in accordance with claim 11, wherein the strip-shaped first
25 ground/power layer is not less than 0.2mm in width.
- 26 13. The substrate in accordance with claim 10, wherein the plurality of openings are
27 formed on the first ground/power layer in radial arrangement.

- 1 14. The substrate in accordance with claim 10, wherein the top surface of the first
2 insulating layer includes a chip-attaching region.
- 3 15. The substrate in accordance with claim 14, further comprising a metal ring formed on
4 the top surface of the first insulating layer between the inner fingers and the
5 chip-attaching region.
- 6 16. The substrate in accordance with claim 15, wherein the metal ring is electrically
7 connected with the first ground /power layer.
- 8 17. The substrate in accordance with claim 10, further comprising a second insulating
9 layer formed on the bottom surface of the first insulating layer to sandwich the first
10 ground/power layer.
- 11 18. The substrate in accordance with claim 17, further comprising a second ground/power
12 layer on the bottom surface of the second insulating layer.
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